Electronic Version
Stylesheet Version v1.1.1

Description

A CMOS Voltage-Controlled Oscillator (VCO) with a Current-Adaptive Resistor for Improved Linearity

Background of Invention

[0001] This invention relates to voltage-controlled oscillators (VCOs), and more particularly for VCO with a current-adaptive resistor.

[0002] Precise clocks are useful in many electronic systems. Clock generator circuits can be adjustable, such as by using a voltage-controlled oscillator (VCO). The frequency of the generated clock can be adjusted by adjusting the voltage that is input to the VCO. Oftentimes the VCO is part of a phase-locked loop (PLL).

[0003] Figure 1 shows a prior-art PLL. A reference clock and a feedback clock are applied to phase detector 10, which compares the edges of the 2 clocks and generates UP and DOWN signals to charge pump 12. Charge pump 12 responds by charging or discharging a loop filter that in-

cludes capacitor 22 and resistor 20. The voltage across the loop filter changes, altering the voltage input to VCO 14. VCO 14 oscillates at a frequency determined by the input voltage from the loop filter.

[0004] Clock driver 16 buffers the output clock from VCO 14 to generate the PLL output clock. The generated clock can be divided by divider 18 before being applied to phase detector 10 as the feedback clock.

[0005] A VCO is commonly used in PLL control systems, including communications, and timing circuitry. Some applications need a wide VCO frequency range with good linearity and high bandwidth.

[0006] One conventional construction for a VCO includes a first portion which converts an input voltage to a control current, and a second portion which converts the control current into an output signal using a ring oscillator. Conventionally the first portion of the VCO is designed to have a linear response in order to effect a linear VCO input/output response. However, this linear control current does not take into account a non-linear current-to-frequency response of the second portion, the ring oscillator.

[0007] In order to reduce power line noise, the conventional construction for a VCO includes a capacitance between a ring

oscillator current-supply node and GND. VCO bandwidth is limited by this capacitance and the effective resistance of the ring oscillator.

[0008] The good linearity and high bandwidth of VCO directly influences the PLL's performance such as reference clock range.

[0009] Many different types of circuits can be used as the VCO. A ring oscillator can be used, and its oscillation frequency changed by adjusting the power-supply voltage applied to the oscillator's gates. A VCO using a current-adaptive resistor is desirable.

Brief Description of Drawings

[0010] Figure 1 shows a prior-art PLL.

[0011] Figure 2 is a schematic diagram of a VCO with a current-adaptive resistor.

[0012] Figure 3A shows frequency response of a prior-art VCO.

[0013] Figure 3B shows frequency response of the VCO with the active resistor.

[0014] Figure 4 is a graph of current through the active resistor and its effective resistance.

Detailed Description

[0015] The present invention relates to an improvement in volt-

age-controlled oscillators (VCOs). The following description is presented to enable one of ordinary skill in the art to make and use the invention as provided in the context of a particular application and its requirements. Various modifications to the preferred embodiment will be apparent to those with skill in the art, and the general principles defined herein may be applied to other embodiments. Therefore, the present invention is not intended to be limited to the particular embodiments shown and described, but is to be accorded the widest scope consistent with the principles and novel features herein disclosed.

[0016] Figure 2 is a schematic diagram of a VCO with a current-adaptive resistor. Current source 60 receives the loop-filter voltage VIN which adjusts as a charge pump charges and discharges a loop filter capacitor in a PLL. The current delivered to the oscillator power-supply OVDD varies with VIN. A higher VIN produces more current from current source 60, raising OVDD. A higher OVDD causes more current to flow in ring oscillator 64, increasing its frequency of operation. OVDD acts as a virtual or internal power-supply to ring oscillator 64.

[0017] Active resistor 62 draws off some of the current from current source 60. This helps to regulate changes in current

flow. The frequency gain of a VCO decreases when VIN increases if the current flowing to the ring oscillator is linear. Active resistor 62 can draw a larger current at low VIN and a smaller current at high VIN. This helps the ring oscillator to get more current at high VIN, adjusting for the non-linear current-to-frequency response of a typical ring oscillator. The source current I_S from current source 60 is split into 2 parallel branches to ground: ring-oscillator current I_O through ring oscillator 64 and resistor current I_R through active resistor 62.

[0018] Since active resistor 62 has both series resistor 42 and series transistor 44 in series, its resistance is not exactly linear, as would be the case for a pure resistor. Instead, series transistor 44 has a transconductance that varies with its drain-to-source voltage. The gate of n-channel series transistor 44 is connected to a fixed bias voltage, NVB, which can be VDD/2 or some other value that can be generated by a voltage divider or other circuit. In one embodiment, NVB can be 1.78v, series resistor 42 is 1.5K-ohm, power (VDD) is 3.3V, and OVDD can vary from 0.8v to 2.4v, depending on the VIN control voltage.

[0019] When the drain voltage of series transistor 44 is less than NVB-Vtn, series transistor 44 operates in the linear re-

gion. Vtn is the threshold voltage of series transistor, and can be 0.5 volts for some processes. When the drain voltage rises above NVB-Vtn, series transistor 44 operates in the saturated region and the current-voltage characteristic of series transistor 44 becomes more non-linear. Thus for higher source currents, which produce higher OVDD, active resistor 62 becomes less linear. This non-linearity at higher OVDD helps to compensate for high-frequency non-linearity of ring oscillator 64. The effective resistance of active resistor 62 increases in the saturated region for higher values of voltage OVDD. This causes a larger fraction of the current to pass through ring oscillator 64 relative to the current through active resistor 62.

[0020] Bypass capacitor 46 is connected between OVDD and ground. Bypass capacitor 46 reduces noise on OVDD, providing a more constant output from the VCO.

[0021] Ring oscillator 64 has an odd number of inverter stages in a loop. The first inverter stage of p-channel transistor 48 and n-channel transistor 50 have drains driving the gates of second-stage transistors 52, 54, which in turn drive the gates of third-stage transistors 56, 58. The drain output of transistors 56, 58 are looped back to the gate input of first-stage transistors 48, 50. The variable-frequency

clock output, OUT, is taken from the drains of third-stage transistors 56, 58. Further buffering can be performed on the output signal.

[0022] Current source 60 has p-channel power transistors 30, 32 with channels in series between the power supply VDD and the oscillator power supply OVDD.

[0023] The gate voltage for lower power transistor 32 is VB, and is generated by the gate and drain of p-channel bias transistor 24, which has its gate and drain connected together. Variable n-channel transistor 34 receives the VCO input voltage VIN, that varies as the loop filter is charged and discharged in the PLL. Tail resistor 38 is connected to the source of variable n-channel transistor 34, while the drain of transistors 24, 34 are connected together as voltage VB. As VIN rises, variable n-channel transistor 34 draws more current, increasing the current pulled through p-channel bias transistor 24, requiring that the gate voltage VB fall. The lower VB increases the source current through power transistor 32, raising OVDD and increasing the frequency of OUT.

[0024] The gate voltage for upper power transistor 30 is VA, which is generated by the drain of p-channel lower bias transistor 28, which receives VB as its gate voltage. The

drain of p-channel lower bias transistor 28 is upper bias voltage VA, which is also applied to the gate of p-channel upper bias transistor 26, which is in series with p-channel lower bias transistor 28 between power and VA.

[0025] Variable n-channel transistor 36 also receives the VCO input voltage VIN, that varies as the loop filter is charged and discharged in the PLL. Tail resistor 40 is connected to the source of variable n-channel transistor 36, while the drain of transistors 28, 36 are connected together as upper bias voltage VA.

[0026] As VIN rises, variable n-channel transistor 36 draws more current, increasing the current pulled through p-channel bias transistors 26, 26, requiring that the gate voltages VA, VB fall. The lower VA, VB increase the source current through power transistor 32, raising OVDD and increasing the frequency of OUT.

[0027] Figure 3A shows frequency response of a prior-art VCO. The prior-art VCO does not have active resistor 62. As the VCO-input voltage VIN is swept from 0.9 to 2.25 volts, curve 68 shows the output frequency of the VCO output. The frequency rises from 200 MHz to almost 2 GHz.

[0028] However, the shape of curve 68 is not a straight line. Instead, frequency rises more rapidly at lower input volt-

ages, while at higher VIN voltages curve 68 flattens out. This curvature of the FREQ-V curve is undesirable. A PLL using this VCO with the response of curve 68 would be somewhat non-linear in response.

[0029] Figure 3B shows frequency response of the VCO with the active resistor. The VCO of Fig. 2 has active resistor 62. As the VCO-input voltage VIN is swept from 0.9 to 2.4 volts, curve 70 shows the output frequency of the VCO output. The frequency rises from 200 MHz to almost 2 GHz.

[0030] Curve 70 is more straight and linear than prior-art curve 68 of Fig. 3A. The more linear FREQ-V curve 70 allows for a PLL to be constructed that has a steady performance over a wide range of reference-clock frequencies. A linear VCO with a large tuning range enables the PLL system to remain stable, and performance is more independent from input frequency, making the PLL more robust Figure 4 is a graph of current through the active resistor and its effective resistance. The current through active resistor 62 of Fig. 2 is not linear as would be the case for a true resistor. Instead, as the voltage OVDD increases from 0.8 to 2.4 volts, the active-resistor current I_R rises sharply initially from 0.8 up to about 1.2 volts. Then the current rises less rapidly from 1.2 volts to 2.4 volts (VDD). Curve 72 shows

that this current rises from about 400 μA to 560 μA.

[0031] The effective resistance, curve 74, rises from about 2 K-ohm to 4.2 K-Ohm over this range. The effective resistance is voltage divided by current, or $OVDD/I_R$. The effective resistance rises with OVDD because of the non-linearity of series transistor 44 in active resistor 62, especially as it enters the saturated region of operation above NVB-Vtn. Noise current from operation of ring oscillator 64 can be shunted through active resistor 62 as well as bypassed by bypass capacitor 46.

[0032] The effective resistance of ring oscillator 64 also varies with OVDD and frequency. At low OVDD and low frequency, the effective resistance of ring oscillator 64 is about 4.5 K-ohms, while at higher OVDD and higher frequency the effective resistance of ring oscillator 64 falls to 0.6 K-ohm.

[0033] The relatively high effective resistance of ring oscillator 64 at low frequency can limit its bandwidth. Bandwidth is limited by the R-C delay of the parallel effective resistances of active resistor 62 and ring oscillator 64, and by the fixed capacitance of bypass capacitor 46. Reducing the effective parallel resistance can reduce the R-C time-constant delay, improving bandwidth.

[0034] However, since active resistor 62 is in parallel with ring oscillator 64, the total resistance is the parallel combination. At low OVDD, ring oscillator 64 has an effective resistance of 4.5K-ohm and active resistor 62 has an effective resistance of 2K-ohm, so the parallel resistance is 4.5K//2K or 1.4 K-ohm. This is much less than the 4.5K-ohm of ring oscillator 64 without active resistor 62. Thus low-frequency performance and bandwidth is improved by adding active resistor 62 in parallel.

[0035] At higher OVDD, ring oscillator 64 has an effective resistance of 0.6K-ohm and active resistor 62 has an effective resistance of 4.2K-ohm, so the parallel resistance is 0.6K//4.2K or 0.5 K-ohm. Overall bandwidth of ring oscillator 64 is thus improved.

[0036] ALTERNATE EMBODIMENTS

[0037] Several other embodiments are contemplated by the inventors. For example, for active resister 62, bias voltage NVB can be connected to a variable voltage to VIN or to OVDD. Rather than use inverters in ring oscillator 64, other kinds of gates such as a NAND gates could be used or could be inserted for resetting. R-C delays could also be added. More than three inverter stages could be used. Other arrangements and circuits for the current source

could be used, and additional devices added such as additional capacitors, resistors, and transistors. Inverters or buffers could be added to the output or to other locations. Various clock drivers could be used. The clock driver could be located after the feedback to the divider.

[0038] Rather than use a current source from power and an active resistor to ground, p-channel and n-channel devices and power and ground could be reversed. Other current-diverting arrangements could be substituted.

[0039] Any advantages and benefits described may not apply to all embodiments of the invention. When the word "means" is recited in a claim element, Applicant intends for the claim element to fall under 35 USC Sect. 112, paragraph 6. Often a label of one or more words precedes the word "means". The word or words preceding the word "means" is a label intended to ease referencing of claims elements and is not intended to convey a structural limitation. Such means-plus-function claims are intended to cover not only the structures described herein for performing the function and their structural equivalents, but also equivalent structures. For example, although a nail and a screw have different structures, they are equivalent structures since they both perform the function of fastening. Claims

that do not use the word "means" are not intended to fall under 35 USC Sect. 112, paragraph 6. Signals are typically electronic signals, but may be optical signals such as can be carried over a fiber optic line.

[0040] The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.